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10/518,608	12/23/2004	Salvatore Pappalardo	02-CT-104/DP	9027

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EXAMINER	
CARTER III, ROBERT E	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,608	PAPPALARDO ET AL.	
	Examiner	Art Unit	
	ROBERT E. CARTER III	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment filed on 11/26/2008 has been entered and considered by the Examiner.

Claim Objections

Claims 1-2 and 5-7 are objected to because of the following informalities: The claims are inconsistent in terminology. Lines 4 and 6-7 of claim 1 and lines 3 and 6-7 of claim 6 claim a "four-terminal inverter". However, lines 8-9 of claim 1, line 2 of claim 2, line 4 of claim 5, lines 4 and 7 of claim 6, and line 1 of claims 7 simply claim "the inverter" or "said inverter". Since there are no other inverters in the claim it is understood that the inverter refers to the four-terminal inverter, however the terminology should be consistent. Either all mentions of "the/said inverter" should be changed to "the/said four-terminal inverter" or mentions of "four-terminal inverter" in lines 6-7 of claim 1 and lines 6-7 of claim 6 should be changed to "the/said inverter". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (Fig. 1) in view of Adam (US Patent # 4,499,388).

As for claim 6, Applicant's admitted prior art (Fig. 1) discloses *A module for driving a row in a liquid crystal display comprising:* *a four-terminal inverter* (T7, T10) *having first* (line between VLCD and T10) *and second* (line between VSS and T7) *power terminals;* *a first* (VLCD) **and** *a second* (VA) *supply voltage; and* *a third* (VB) **and** *fourth* (VSS) *supply voltage, wherein the inverter includes an input* (gates of T7 and T10) *driven by a logic circuit* (1) *and further includes an output* (OUT) *which provides a drive signal for the row* (Page 3, line 28 – Page 4, line 9).

Applicant's admitted prior art (Fig. 1) does not teach an inverter operating between two switches.

In the same field of endeavor (i.e. four voltage level selection circuits) Adam (Figs. 1a, 2, 3) discloses:

A module comprising:

a four-terminal logic inverter (T21, T22) *having first* (line between T11, T12, and T22) *and second* (U) *power terminals;*

a first switch (T11, T12) *for coupling the first power terminal of the four-terminal inverter to a first* (U3) *or a second* (U1) *supply voltage; and*

a second switch (MT, ZT) *for coupling the second power terminal of the inverter to a third* (U2) *or fourth* (U0) *supply voltage, wherein the inverter includes an input* (gates of T21 and T22) *driven by a logic circuit* (Fig. 3)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the four voltage selection circuit for driving an LCD row in Applicant's admitted prior art (Fig. 1) with the four voltage selection circuit in Adam to reduce the output resistance of the selection circuit (Adam, Col. 1, lines 38-42).

Applicant's admitted prior art (Fig. 1) as modified by Adam does not teach the first power terminal, the second power terminal, the input and the output being separate terminals.

In the same field of endeavor (i.e.) logic controlled selection circuits) Zukowski teaches a circuit composed of 3 cascaded 2-1 multiplexers which selects one of 4 inputs and connects it to the output (Fig. 1D, Col. 2, lines 49-55). As can be seen from Fig. 1D, Zukowski clearly teaches the output 2-1 multiplexer #18 having a first input terminal (output from top 2-1 MUX #17), a second input terminal (output from bottom 2-1 MUX #17), a control input terminal #19, and an output terminal Y, all being separate terminals.

2-1 multiplexers and inverters may have different internal structure but operate in a well known and identical manner from a logic standpoint. They both have a first and second input terminal, one control input terminal, and one output terminal. When the control input terminal voltage is low, one of the input terminals is selected and connected to the output terminal. When the control input terminal voltage is high, the other input terminal is selected and connected to the output terminal.

Therefore, because both Applicant's admitted prior art (Fig. 1) as modified by Adam, and Zukowski, teach structures for switching 4 inputs to one output, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute one switching structure for the other to achieve the predictable result of selecting a voltage and connecting it to the output.

Furthermore, because 2-1 multiplexers and inverters perform identically from a logic standpoint, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute inverters for the 2-1 multiplexers of Zukowski predictable result of selecting a voltage and connecting it to the output.

Therefore Applicant's admitted prior art (Fig. 1) as modified by Adam and Zukowski teaches all the limitations of claim 6, including *the first power terminal, the second power terminal, the input and the output being separate terminals.*

As for claim 1, this claim recites the same limitations as claim 6 above, and therefore is rejected as per claim 6 above. Claim 1 differs from claim 6 in that the limitations of first and second supply lines are additionally recited. The limitations "a first

and a second supply line" is taught by Adam as previously addressed in claim 6 (i.e. inverter, power terminals, switches)

Adam teaches these limitations as outlined below:

a four-terminal logic inverter (T21, T22) *operating in a supply path between a first* (T11, T12, line between T11, T12, and T22) *and a second* (MT, ZT, T21) *supply line of said system, said first supply line comprising a first switch* (T11, T12) *...and said second supply line comprising a second switch* (MT, ZT)

As for claim 2, Applicant's admitted prior art (Fig. 1) as modified by Adam teaches:

wherein said inverter comprises a PMOS transistor (Adam, T21) *and a NMOS transistor* (Adam, T22).

As for claim 7, this claim recites the same limitations as claim 2 above, and therefore is rejected as per claim 2 above.

As for claim 8, Adam teaches:

wherein the first and second supply voltages have different values, and the third and fourth supply voltages have different values (Col. 3, lines 6-15, 36-40).

As for claim 3, Applicant's admitted prior art (Fig. 1) teaches:

wherein the value of said first supply voltage (VLCD) *exceeds said second supply voltage* (VA)*, and the value of said second supply voltage exceeds said third supply voltage* (VB)*, and the value of said third supply voltage exceeds said fourth supply voltage* (VSS), (See (Fig. 1), Page 3, line 28 – Page 4, line 9).

As for claim 4, Applicant's admitted prior art (Fig. 1) teaches:

a logic signal (LOW_FRAME) *that controls respectively the connection of the first or second supply voltage and the connection of the third or fourth supply voltage according to whether a frame is uneven or even* (See (Fig. 1), Page 2, lines 14-24).

Adam et al. teaches:

wherein said first and second switches are controlled by a logic signal (A, B) *that controls respectively the connection of the first supply line to said first or to said second supply voltage and the connection of the second supply line to said third or to said fourth supply voltage* (Col. 3, lines 26-32).

Combining applicant's admitted prior art and Adam meet the claim limitations.

As for claim 5, Applicant's admitted prior art (Fig. 1) teaches:

wherein said logic circuitry (1, C1) *comprises a logic device* (1) *capable of supplying an additional input logic signal* (A) *to an elevator device* (C1) *capable of raising the level of said additional logic signal for driving said inverter* (See (Fig. 1), Page 2, lines 14-24).

As for claim 9, Applicant's admitted prior art (Fig. 1) as modified by Adam teaches:

wherein the first and second switches are driven by a logic signal, the state of the logic signal being determined by whether a frame is uneven or even (Applicant's admitted prior art (Fig. 1) [0008]).

As for claim 10, Applicant's admitted prior art (Fig. 1) teaches:

further comprising a level shifter (See (Fig. 1), Page 2, lines 14-24).

Response to Arguments

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT E. CARTER III whose telephone number is (571)270-3006. The examiner can normally be reached on 9AM - 5:30PM Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/R.E.C./